LOW VOLTAGE/LOW POWER DESIGN IN FUTURE NODES

There is a golden law in semiconductor industry called Moore's law. It states that the number of transistors on a given area of silicon doubles every two years. When Moore came up with his "law" back in 1965, he had in mind a design of about 50 components. Today's chips consist of billions of transistors and design teams strive for "better, sooner, cheaper" products with every new process node. To achieve the large increases in levels of integration, many parameters have changed. Fundamentally the feature sizes have reduced to enable more devices to be fabricated within a given area. However other figures such as power dissipation, and line voltage have reduced along with increased frequency performance. The basic tenet of Moore's law has held true for many years from the earliest years of integrated circuit technology. However, there are limits to the scalability of the individual devices and as process technologies continued to shrink towards 20 nm, it became impossible to achieve the proper scaling of various device parameters. It was found that optimizing for one variable such as performance resulted in unwanted compromises in other areas like power. It was therefore necessary to look at other more revolutionary options like a change in transistor structure from the traditional planar transistor.

FinFET technology has been born as a result of the relentless increase in the levels of integration. Modern FinFETs are 3D structures that rise above the planar substrate, giving them more volume than a planar device for the same planar area. Given the excellent control of the conducting channel by the gate, which "wraps" around the channel, very little current is allowed to leak when the device is in the off state. This allows the use of lower voltages, which results in optimal switching speeds and power.

FinFET processes are already in production. Intel was one of the first semiconductor manufacturers to use the 22nm node, where it re-

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ported power savings of up to 50% when compared to its 32nm process. While Intel started using FinFET technology at 22nm, most foundries are expected to adopt FinFETs at 16nm or 14nm. Like any new technology introduction, however, 16/14nm FinFETs pose some design challenges. Most of these challenges are on the custom/analog side, but there are also issues that digital designers need to be aware of.

Custom designers working with standard cells, and analog designers working on IP blocks, will notice some changes with FinFETs. In particular, some of the design strategies they have used in the past will no longer work. This is because the intrinsic device characteristics are different. For instance, with planar transistors, standard cell designers can arbitrarily change transistor width in order to manage drive current. With FinFETs, designers cannot do this – they can only add or subtract fins to change the drive current. Fins come in discrete increments – you can't add three-quarters of a fin. This issue is sometimes called "width quantization." Therefore, FinFET processes will require some changes to custom/analog and digital implementation flows.

In this project, FinFET devices are utilized for custom/analog and digital blocks in both circuit and device level designs. Also, we will investigate FinFET and its potentials for low-power applications and design some analoge and mixed-signal building blocks by FinFET in sub 14-nm technologies using the Design Kits provided by IMEC.

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